Amendments to the Claims:

1.   (Currently Amended) A data processing system having:

at least one processor chip including a processor unit and an internal data cache, and

an interface external to the internal data cache and external to the processor chip, and configured to receive cache mirror data from the processor chip, the interface further configured to discard all the cache mirror data to be written to an external memory received from the processor chip so that cache mirror data is never written to external memory during operation of the processor chip.

2.   (Previously Presented) A data processing system according to claim 1 in which the interface is coupled to a memory, the interface passing data to the processor chip during initialization.

3.   (Original) A data processing system according to claim 1 further including one or more further processing chips which have read/write access to external memory.

4.   (Currently Amended) A method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting cache mirror data write instructions out of the processing chip, the method including discarding the write instructions at an interface external to the processing chip so that cache mirror data is never written to external memory during operation of the processing chip, the external interface providing a connection between the processing chip and an address controller; and arranging for the program code operated by the processor to require only the data cache as memory.

5.   (Previously Presented) A data processing system according to claim 1 wherein the at
least one processor chip comprises exactly one processor chip.

6.   (Previously Presented) A data processing system according to claim 1 wherein the at
least one processor chip comprises two processor chips.

7.   (Previously Presented) A data processing system according to claim 1 wherein the
processor chip further includes an internal cache controller coupled between the internal data
cache and the processor unit.

8.   (Currently Amended) A data processing system comprising:
        a processor chip including an internal processor coupled to an internal data cache;
        an external memory;
        an address decoder; and
        an interface external to the internal data cache and external to the processor chip, the
interface coupled between the processor chip and the external memory and providing the only
connection between the processor chip and the address decoder, the interface configured to
receive memory data from the external memory and transfer the memory data to the processor
chip, the interface further configured to receive internal data cache mirror data from the
processor chip and discard all the internal data cache mirror data to be written to the external
memory so that the internal data cache mirror data is never written to external memory.

9.   (Previously Presented) The system of claim 8 and further comprising a control circuit coupled to the interface circuit, the control circuit providing a control signal to indicate whether data received by the interface should be discarded.

10.   (Previously Presented) The system of claim 9 wherein the control circuit comprises a decoder.

11.   (Previously Presented) The system of claim 8 and further comprising:

    a second processor chip that includes an internal processor coupled to an internal cache; and

    a second interface, wherein the second processor chip is coupled to the external memory through the second interface.

12.   (Previously Presented) The system of claim 11 and further comprising a system bus coupled to the processor chip, the second processor chip, the interface, and the second interface.

13.   (Previously Presented) The system of claim 12 and further comprising a third processor chip coupled to the system bus.

14.   (Previously Presented) The system of claim 13 wherein the third processor chip comprises a master processing unit and wherein the processor chip and the second processor chip comprise slave processing units.

15.   (Previously Presented) The system of claim 14 and further comprising a second external memory directly coupled to the system bus.

16.   (Currently Amended) A method of operating a data processing system having a plurality of integrated circuits, each integrated circuit having a processor, an internal data cache, and a cache controller, the method comprising:

transmitting cache mirror data write instructions from a first cache controller of a first integrated circuit to an external memory interface, wherein the external memory interface is located outside the first integrated circuit, the external memory interface not operating as a data cache; and

discarding the first cache mirror data write instructions at the external memory interface so that cache mirror data is never written to external memory during operation of the first processor.

17.   (Previously Presented) The method of claim 16, further comprising:

transmitting second cache mirror data write instructions from a second cache controller in a second integrated circuit to the external memory interface;

writing the second cache mirror data write instructions from the external memory interface to external memory.

18.   (Previously Presented) The method of claim 17, further comprising:

determining if a task requires a read/write memory that is larger than an internal data cache size; and

allocating the task to the first integrated circuit or to the second integrated circuit based upon the determining step.